Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) An apparatus ~~Apparatus (10; 20; 70; 90; 100)~~ comprising a level shifter ~~(15; 75; 95; 103)~~ connectable to a signal input ~~(1; 31; 71; 91)~~ for receiving an input signal ~~(s(t))~~ with a negative signal swing, said level shifter ~~(15; 75; 95; 103)~~ providing for a DC shift of said input signal ~~(s(t))~~ to provide an output signal ~~(r(t))~~ with positive signal swing, said level shifter ~~(15; 75; 95; 103)~~ comprising: an amplifier ~~(17; 77)~~ having a first input ~~(11; 61)~~, a second input ~~(12; 62)~~, and an output ~~(13; 73)~~, a first capacitor ~~(C1)~~, a second capacitor ~~(C2; C2A, C2B to C2n)~~, a reference voltage supply ~~(16; 79)~~, and a transistor ~~(14; 74)~~ serving as a switch, wherein said first capacitor ~~(C1)~~ is arranged between said signal input ~~(1; 71; 91)~~ and said first input ~~(11; 61)~~, said second capacitor ~~(C2; C2A, C2B to C2n)~~ is arranged in a feedback-loop ~~(18)~~ between the output ~~(13; 73)~~ and said first input ~~(11; 61)~~, said reference voltage supply ~~(16; 79)~~ is connectable to said second input ~~(12; 62)~~, and wherein said transistor ~~(14; 74)~~ is arranged in a branch ~~(19; 69)~~ that bridges the second capacitor ~~(C2; C2A, C2B to C2n)~~, whereby a control signal ~~(CNTRL)~~ is applicable to a gate ~~(14.1; 74.1)~~ of said transistor ~~(14; 74)~~ in order to allow the level shifter ~~(15; 75; 95; 103)~~ to be reset from time to time.

2. (currently amended) The apparatus of claim 1, wherein the gain of the amplifier ~~(17; 77)~~ is adjustable by varying the effective capacitance of the capacitors ~~(C2; C2A, C2B to C2n)~~.

3. (currently amended) The apparatus of claim 2, wherein a branch that bridges the second capacitor is provided, said branch comprising a capacitor ~~(C2B, C2n)~~ in series with a switch ~~(sb, sn)~~, whereby the effective capacitance can be varied by opening or closing the switch ~~(sb, sn)~~.

4. (currently amended) The apparatus of claim 2, comprising an analog-to-digital converter ~~(80)~~ connectable to the output ~~(73)~~ for determining the voltage level at the output ~~(73)~~, and a controller ~~(78; 96)~~ for receiving digital information from to the analog-to-digital converter ~~(80)~~, said digital information representing the voltage level, said controller ~~(78; 96)~~ providing a signal to adjust the effective capacitance.

5. (currently amended) The apparatus of claim 1, comprising a digital-to-analog converter ~~(79)~~ serving as reference voltage supply, said digital-to-analog converter ~~(79)~~ preferably receiving a digital signal from a controller ~~(78; 96)~~.

6. (currently amended) The apparatus of claim 1, comprising a bias current source ~~(21; 93)~~ with a network having a plurality of transistors ~~(P1, P2, P3)~~, resistors ~~(R1, R2)~~, and a reference current source ~~(22)~~.

7. (currently amended) The apparatus of claim 6, wherein one of the transistors is a cascode transistor ~~(P3)~~ which is arranged with respect to one of the other transistors ~~(P2)~~ so as to absorb any voltage beyond a supply voltage ~~(Vsupply)~~, if the input signal ~~s(t) at~~ falls below 0V.

8. (currently amended) The apparatus according to claim 1, further comprising ESD protection means ~~(92)~~ being adapted to handle negative voltage swings at the signal input ~~(91)~~.

9. (currently amended) The apparatus of claim 8, wherein the ESD protection means ~~(92)~~ comprise a first diode ~~(DP2)~~, a second diode ~~(DP1)~~, and a third diode ~~(DCL1)~~, said first diode ~~(DP2)~~ being situated between the signal input ~~(91)~~ and a supply node ~~(101)~~, said second diode ~~(DP1)~~ being situated between the supply node ~~(101)~~ and a substrate ~~(102)~~, and said third diode ~~(DCL1)~~ being situated between the supply node ~~(101)~~ and the substrate ~~(102)~~.